

CLAIMS

What is claimed is:

1. A method for forming a MOS transistor having elevated source and drain structures, comprising:
 - 5 providing a sacrificial gate pattern on a substrate;
 - providing an epitaxial layer on the substrate adjacent the sacrificial gate pattern;
 - providing a first insulating layer and a second insulating layer on the epitaxial layer adjacent the sacrificial gate pattern;
 - removing the sacrificial gate pattern to expose a portion of the substrate and wall portions of the epitaxial layer;
 - 10 providing a gate dielectric layer on the exposed portion of the substrate and along the wall portions of the epitaxial layer;
 - providing a gate electrode on the gate dielectric layer;
 - removing the second insulating layer and the first insulating layer;
 - 15 doping the epitaxial layer with impurities using the gate electrode as a mask to form source/drain extension regions in the epitaxial layer proximal to the gate dielectric layer;
 - providing insulating spacers on sidewalls of an upper portion of the gate electrode; and
 - 20 doping the epitaxial layer with impurities using the gate electrode and insulating spacers as a mask to form deep source/drain regions adjacent the source/drain extension regions.
2. The method of claim 1 wherein the source/drain extension regions are formed by doping the epitaxial layer with impurities prior to providing the silicon nitride film and silicon oxide film on the epitaxial layer.
- 25 3. The method of claim 1 wherein providing the sacrificial gate pattern comprises sequentially forming a silicon oxide film and a silicon nitride film and patterning the

sequentially formed films to form the sacrificial gate pattern.

4. The method of claim 1 wherein the substrate is of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI);
5 strained silicon; strained silicon-on-insulator; and GaAs.
5. The method of claim 1 further comprising forming a pad oxide layer on the epitaxial layer.
- 10 6. The method of claim 1 wherein providing a first insulating layer and a second insulating layer on the epitaxial layer adjacent the sacrificial gate pattern comprises:
sequentially providing a silicon nitride film and a silicon oxide film on the epitaxial layer and the sacrificial gate pattern;
planarizing the silicon nitride film, silicon oxide film and sacrificial gate pattern
15 to expose an upper surface of the sacrificial gate pattern;
7. The method of claim 6 wherein planarizing comprises planarizing by a chemical-mechanical polishing process (CMP) or an etch-back treatment.
- 20 8. The method of claim 1 wherein removing the sacrificial gate pattern comprises etching the sacrificial gate pattern to expose an upper surface of the substrate.
9. The method of claim 1 wherein removing the sacrificial gate pattern comprises etching the sacrificial gate pattern to form a recess in the substrate.
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10. The method of claim 9 wherein providing the gate dielectric layer comprises providing the gate dielectric layer on bottom and side walls of the recess of the substrate.
11. The method of claim 9 wherein the recess is of a depth that is less than 50nm.
- 30 12. The method of claim 1 further comprising doping the exposed portion of the substrate

with impurities to form a channel region following removal of the sacrificial gate pattern.

13. The method of claim 1 further comprising doping a channel region of the substrate with impurities prior to providing the sacrificial gate pattern on the substrate.

14. The method of claim 1 wherein the gate dielectric layer comprises a material selected from the group of materials consisting of: silicon oxide film; silicon oxy-nitride (SiON); tantalum oxide; and a high-dielectric-constant material.

15. The method of claim 1 wherein providing the gate dielectric layer comprises forming the gate dielectric layer using a deposition or thermal oxidation process.

16. The method of claim 1 wherein providing the gate electrode comprises:
forming a gate electrode material film on the gate dielectric layer and the silicon oxide film;
planarizing the gate electrode material film and silicon oxide film.

17. The method of claim 16 wherein planarizing comprises planarizing by a chemical-mechanical polishing process (CMP) or an etch-back treatment.

18. The method of claim 1 wherein the gate electrode comprises a material selected from the group of materials consisting of polysilicon film; silicon germanium film; silicide film; metal film; and a laminate film.

19. The method of claim 1 wherein removing the second insulating layer and first insulating layer comprises removing using a wet etching process.

20. The method of claim 1 wherein providing insulating spacers on sidewalls of an upper portion of the gate electrode comprises:

providing a silicon nitride film on the resultant structure; and
anisotropically etching the silicon nitride film.

21. The method of claim 20 further comprising, prior to providing the silicon nitride film, providing a silicon oxide buffer layer on the resultant structure.

22. The method of claim 1 further comprising forming a silicide film on the source/drain regions and the gate electrode.

23. The method of claim 22, wherein the silicide film comprises a material selected from a group consisting of Co, Ni, W, Ti and combinations thereof.

24. The method of claim 1 wherein the depth of the source/drain extension regions is less than the depth of the deep source/drain regions.

25. The method of claim 1 wherein the deep source/drain regions extend into the substrate.

26. The method of claim 1 wherein the source/drain extension regions extend into the substrate.

27. A MOS transistor having elevated source and drain structures, comprising:

a gate dielectric layer on a substrate;

a gate electrode on the gate dielectric layer;

an epitaxial layer adjacent the gate dielectric layer on the substrate;

first source/drain regions in the epitaxial layer adjacent the gate dielectric layer at lower side portions of the gate electrode; and

insulating spacers on the epitaxial layer at an upper side portion of the gate electrode.

28. The transistor of claim 27 wherein the gate dielectric layer extends across a bottom portion and the lower side portions of the gate electrode;

29. The transistor of claim 27 wherein the first source/drain regions are formed by doping the

epitaxial layer with impurities:

30. The transistor of claim 27 further comprising second source/drain regions adjacent the first source/drain regions opposite the gate electrode .
- 5 31 The transistor of claim 29 wherein the second source/drain regions are formed by doping exposed surfaces with impurities using the gate electrode and insulating spacers as a mask.
- 10 32. The transistor of claim 29 wherein the first source/drain regions comprise source/drain extension regions and wherein the second source/drain regions comprise deep source/drain regions.
- 15 33. The transistor of claim 29 wherein the depth of the first source/drain regions is less than the depth of the second source/drain regions.
34. The transistor of claim 29 wherein the second source/drain regions extend into a portion of the substrate.
- 20 35. The transistor of claim 29 wherein the first source/drain regions extend into a portion of the substrate.
- 25 36. The transistor of claim 27 wherein the substrate is formed of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.
37. The transistor of claim 27 wherein the epitaxial layer comprises silicon or silicon germanium.
- 30 38 The transistor of claim 27 wherein the gate dielectric layer and gate electrode extend into a trench formed in an upper portion of the substrate.

39. The transistor of claim 38 wherein the trench is of a depth that is less than 50nm.

40. The transistor of claim 27 further comprising a channel region in the substrate under the
5 gate electrode and adjacent the lower side portions of the gate electrode.

41. The transistor of claim 27 wherein the gate dielectric layer comprises a material selected
from the group of materials consisting of: silicon oxide film; silicon oxy-nitride (SiON);
tantalum oxide; and a high-dielectric-constant material.

10 42. The transistor of claim 27 wherein the gate dielectric layer is formed using a deposition
or thermal oxidation process.

15 43. The transistor of claim 27 wherein the gate electrode comprises a material selected from
the group of materials consisting of polysilicon film; silicon germanium film; silicide film;
metal film; and a laminate film.

44. The transistor of claim 27 further comprising a silicon oxide buffer layer between the
gate electrode and the insulating spacers.

20 45. The transistor of claim 27 further comprising a silicide film on the source/drain regions
and the gate electrode.

25 46. The transistor of claim 45, wherein the silicide film comprises a material selected from a
group consisting of Co, Ni, W, Ti and combinations thereof.

47. A MOS transistor having elevated source and drain structures, comprising:
 a gate dielectric layer on a substrate;
 a gate electrode on the gate dielectric layer, wherein the gate dielectric layer
 extends across a bottom portion and lower side portions of the gate electrode;
 an epitaxial layer adjacent the gate dielectric layer on the substrate;
 first source/drain regions in the epitaxial layer adjacent the gate dielectric layer at
 the lower side portions of the gate electrode; and
 second source/drain regions adjacent the first source/drain regions opposite the
 gate electrode.

48. The transistor of claim 47 wherein the first source/drain regions are formed by doping the
 epitaxial layer with impurities.

49. The transistor of claim 47 further comprising insulating spacers on the epitaxial layer at
 an upper side portion of the gate electrode, wherein the second source/drain regions are
 formed by doping exposed surfaces with impurities using the gate electrode and
 insulating spacers as a mask.

50. The transistor of claim 49 wherein the first source/drain regions comprise source/drain
 extension regions and wherein the second source/drain regions comprise deep
 source/drain regions.

51. The transistor of claim 47 wherein the substrate is of a type selected from the group
 consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI);
 strained silicon; strained silicon-on-insulator; and GaAs.

52. The transistor of claim 47 wherein the first source/drain regions are formed to a first
 depth in the epitaxial layer and wherein the second source/drain regions are formed to a
 second depth, wherein the first depth is less than the second depth.

53. The transistor of claim 47 wherein the second source/drain regions extend into a portion

of the substrate.

54. A MOS transistor having elevated source and drain structures, comprising:

a substrate having a trench in an upper portion thereof;

a gate dielectric layer lining the trench;

a gate electrode on the gate dielectric layer, the gate electrode extending into the trench, wherein the gate dielectric layer extends across a bottom portion and lower side portions of the gate electrode;

an epitaxial layer adjacent the gate dielectric layer on the substrate;

first source/drain regions in the epitaxial layer adjacent the gate dielectric layer at the lower side portions of the gate electrode; and

second source/drain regions adjacent the first source/drain regions opposite the gate electrode .

55. The transistor of claim 54 wherein the first source/drain regions are formed by doping the epitaxial layer with impurities.

56. The transistor of claim 54 further comprising insulating spacers on the epitaxial layer at an upper side portion of the gate electrode, wherein the second source/drain regions are formed by doping exposed surfaces with impurities using the gate electrode and insulating spacers as a mask.

57. The transistor of claim 56 wherein the first source/drain regions comprise source/drain extension regions and wherein the second source/drain regions comprise deep source/drain regions.

58. The transistor of claim 54 wherein the substrate is of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

59. The transistor of claim 54 wherein the first source/drain regions are formed to a first

depth in the epitaxial layer and wherein the second source/drain regions are formed to a second depth, wherein the first depth is less than the second depth.

60. The transistor of claim 54 wherein the second source/drain regions extend into a portion of the substrate.

61. The transistor of claim 54 wherein the first source/drain regions extend into a portion of the substrate.

62. A MOS transistor having elevated source and drain structures, comprising:

a gate dielectric layer on a substrate;

a gate electrode on the gate dielectric layer, wherein the gate dielectric layer extends across a bottom portion and lower side portions of the gate electrode;

an epitaxial layer adjacent the gate dielectric layer on the substrate;

source/drain extension regions in the epitaxial layer adjacent the gate dielectric layer at the lower side portions of the gate electrode formed by doping the epitaxial layer with impurities;

insulating spacers on the epitaxial layer at an upper side portion of the gate electrode; and

deep source/drain regions adjacent the source/drain extension regions opposite the gate electrode, wherein the deep source/drain regions are formed by doping the epitaxial layer with impurities using the gate electrode and insulating spacers as a mask.

63. The transistor of claim 62 wherein the substrate is of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

64. The transistor of claim 62 wherein the deep source/drain regions extend into the substrate under the epitaxial layer.

65. The transistor of claim 62 wherein the source/drain extension regions extend into a

portion of the substrate.

66. The transistor of claim 62 wherein the gate electrode extends into a trench formed in an upper portion of the substrate.

67. A MOS transistor having elevated source and drain structures, comprising:

a substrate having a trench in an upper portion thereof;

a gate dielectric layer lining the trench;

a gate electrode on the gate dielectric layer, the gate electrode extending into the trench, wherein the gate dielectric layer extends across a bottom portion and lower side portions of the gate electrode;

an epitaxial layer adjacent the gate dielectric layer on the substrate;

source/drain extension regions in the epitaxial layer adjacent the gate dielectric layer at the lower side portions of the gate electrode formed by doping the epitaxial layer with impurities;

insulating spacers on the epitaxial layer at an upper side portion of the gate electrode; and

deep source/drain regions adjacent the source/drain extension regions opposite the gate electrode, wherein the deep source/drain regions are formed by doping the epitaxial layer with impurities using the gate electrode and insulating spacers as a mask.

68. The transistor of claim 67 wherein the substrate is of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

69. The transistor of claim 67 wherein the deep source/drain regions extend into the substrate under the epitaxial layer.

70. The transistor of claim 67 wherein the source/drain extension regions extend into the substrate under the epitaxial layer.

71. The transistor of claim 67 wherein the trench is of a depth that is less than 50nm.

72. A MOS transistor having elevated source and drain structures, comprising:

a gate dielectric layer on a substrate;

a gate electrode on the gate dielectric layer, wherein the gate dielectric layer extends across a bottom portion and lower side portions of the gate electrode;

an epitaxial layer adjacent the gate dielectric layer on the substrate; and

first source/drain regions in the epitaxial layer adjacent the gate dielectric layer at lower side portions of the gate electrode.

73. The transistor of claim 72 further comprising insulating spacers on the epitaxial layer at an upper side portion of the gate electrode.

74. The transistor of claim 72 wherein the gate dielectric layer extends across a bottom portion and the lower side portions of the gate electrode;

75. The transistor of claim 72 wherein the first source/drain regions are formed by doping the epitaxial layer with impurities.

76. The transistor of claim 72 further comprising second source/drain regions adjacent the first source/drain regions opposite the gate electrode .

77. The transistor of claim 72 wherein the second source/drain regions are formed by doping exposed surfaces with impurities using the gate electrode and insulating spacers as a mask.

78. The transistor of claim 76 wherein the first source/drain regions comprise source/drain extension regions and wherein the second source/drain regions comprise deep source/drain regions.

79. The transistor of claim 76 wherein the depth of the first source/drain regions is less than

the depth of the second source/drain regions.

80. The transistor of claim 76 wherein the second source/drain regions extend into a portion of the substrate.

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81. The transistor of claim 76 wherein the first source/drain regions extend into a portion of the substrate.

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82. The transistor of claim 72 wherein the substrate is formed of a type selected from the group consisting of: silicon; silicon-on-insulator (SOI); SiGe; SiGe-on-insulator(SGOI); strained silicon; strained silicon-on-insulator; and GaAs.

83. The transistor of claim 72 wherein the epitaxial layer comprises silicon or silicon germanium.

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84. The transistor of claim 72 wherein the gate dielectric layer and gate electrode extend into a trench formed in an upper portion of the substrate.

85. The transistor of claim 84 wherein the trench is of a depth that is less than 50nm.

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86. The transistor of claim 72 further comprising a channel region in the substrate under the gate electrode and adjacent the lower side portions of the gate electrode.

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87. The transistor of claim 72 wherein the gate dielectric layer comprises a material selected from the group of materials consisting of: silicon oxide film; silicon oxy-nitride (SiON); tantalum oxide; and a high-dielectric-constant material.

88. The transistor of claim 72 wherein the gate dielectric layer is formed using a deposition or thermal oxidation process.

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89. The transistor of claim 72 wherein the gate electrode comprises a material selected from

the group of materials consisting of polysilicon film; silicon germanium film; silicide film; metal film; and a laminate film.

- 5 90. The transistor of claim 72 further comprising a silicon oxide buffer layer between the gate electrode and the insulating spacers.
91. The transistor of claim 72 further comprising a silicide film on the source/drain regions and the gate electrode.
- 10 92. The transistor of claim 72, wherein the silicide film comprises a material selected from a group consisting of Co, Ni, W, Ti and combinations thereof.